

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent: 6,475,846

Date of Issue: November 5, 2002

Name of Patentee: Marotta et al.

Title of Invention: METHOD OF MAKING FLOATING-GATE MEMORY-CELL ARRAY
WITH DIGITAL LOGIC TRANSISTORS

PROPOSED DRAWING AMENDMENT UNDER 37 CFR §1.173(b)(3)

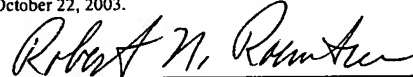
October 22, 2003

Box REISSUE

Assistant Commissioner for Patents

Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the
U.S. Postal Service as First Class Mail in an envelope addressed to:
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October 22, 2003.



Robert N. Rountree, Reg. No. 39,347

Dear Sir:

Please change the Vdd label of Figure 1 at the source of transistor 27 to Ground in agreement with the Ground symbol as marked in red on the attached figure. Two paragraphs from column 4 of the specification are amended to agree with the drawing amendment. No new matter is added.

Respectfully submitted,



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